

## CLAIMS

### I Claim:

- 1 1. A method of accessing data in a data processing system having a graphics engine, the  
2 method comprising:  
3 accessing a first portion of a frame of graphics data through a first channel  
4 of memory;  
5 accessing a second portion of a frame of graphics data through a second  
6 channel of memory;  
7 accessing system data through the first channel of memory simultaneously  
8 with the step of accessing the second portion of a frame of graphics  
9 data through the second channel of memory.
- 1 2. The method of claim 1, wherein the first portion and second portion are logically  
2 consecutive blocks of graphics data.
- 1 3. The method of claim 2, wherein the logically consecutive blocks are for storing  
2 horizontally adjacent pixel matrices.
- 1 4. The method of claim 2, wherein the logically consecutive blocks are for storing  
2 vertical adjacent pixel matrices.
- 1 5. The method of claim 1, wherein the first channel accesses data on first clock edge, and  
2 the second channel accesses data on a second clock edge, wherein the first clock  
3 edge and the second clock edge are skewed from one another.

1 6. The method of claim 1, wherein:

2 the step of accessing the first portion of a frame of graphics data through a first  
3 channel includes the first portion being a first type of graphics memory;  
4 the step of accessing a second portion of a frame of graphics data through a  
5 second channel includes the second portion being a second type of  
6 graphics memory;

1 7. The method of claim 6, wherein the step of accessing the first portion and the step of  
2 accessing a second portion are performed substantially simultaneously.

1 8. The method of claim 6, wherein the first portion of a frame of graphics data and the  
2 second portion of a frame of graphics data are associated with a common pixel.

1 9. The method of claim 6, wherein the first type is z graphics data, and the second type is  
2 destination graphics data.

1 10. A method of partitioning memory in a data processing system, the method  
2 comprising:  
3 identifying a first portion of a memory associated with a first channel as graphics  
4 memory;  
5 identifying a second portion of a memory associated with a second channel as  
6 graphics memory;  
7 partitioning each of the first and a second portion of memory into blocks;  
8 mapping each of the blocks to an X-Y location, wherein each block associated  
9 with a first channel is horizontally and vertically adjacent to blocks  
10 associated with the second channel.

1 11. A method of accessing data in a data processing system, the method comprising the  
2 steps of:

3 storing a first data to one of a first memory and a second memory, wherein the  
4 first memory is associated with a first memory channel, the second  
5 memory is associated with a second memory channel, and the first data is  
6 associated with a first location of a video image and has a first video data  
7 type.

8 storing a second data to one of the first and second memory, wherein the second  
9 data is associated with the first location of the video image and has a  
10 second video data type, and is stored in a different memory than the first  
11 data.

1 12. The method of claim 11, wherein the first data type is a Z-data associated with a  
2 three-dimensional image.

1 13. The method of claim 12, wherein the second data type is a destination (DST) data  
2 associated with a three-dimensional image.

1 14. The method of claim 11, further comprising the steps of:

2 storing a third data to one of the first and second memory, wherein the third data  
3 is associated with a second location of a video image, has the first video  
4 data type, and is stored in a different memory than the first data.

5 storing a fourth data to one of the first and second memory, wherein the second  
6 data is associated with the second location of the video image, has the  
7 second video data type, and is stored in a different memory than the third  
8 data.

10075449-034403

1 15. A method of partitioning data, the method comprising:  
2 determining the memory present in a system;  
3 partitioning the memory between a first channel and a second channel;  
4 partitioning a first portion of the memory associated with the first channel as  
5 system memory;  
6 partitioning a second portion of the memory associated with the first channel as  
7 graphics memory; and  
8 partitioning at least a portion of the memory associated with the second channel as  
9 graphics memory.

1 16. The method of claim 15, wherein the graphics memory associated with the first  
2 channel and the graphics memory associated with the second channel are arranged  
3 in blocks of data having adjacent physical addresses.

1 17. The method of claim 16, wherein the adjacent physical addresses are arranged in  
2 rows and columns so that each block associated with a row and column is adjacent  
3 to a block accessed by a different channel.

1 18. A data processing system comprising:  
2 a system controller having:  
3 a first memory channel controller;  
4 a second memory channel controller; and  
5 a high-speed PCI bus arbiter;  
6 an input output (IO) controller coupled to the high-speed PCI bus arbiter, and  
7 having a low-speed PCI bus arbiter, wherein the low speed PCI arbiter  
8 supports a slower PCI bus rate than the high-speed PCI bus arbiter.

1 19. The system of claim 18, wherein a bus rate of the high speed PCI bus arbiter is at  
2 least 10 percent faster than the bus rate of the low speed PCI bus arbiter.

1 20. The system of claim 19, wherein the bus rate of the high speed PCI bus arbiter is  
2 approximately 66 Mbits per second per data pin and the bus rate of the low speed  
3 PCI bus arbiter is approximately 33 Mbits per second per data pin.

1 21. The system of claim 18, further comprising a data storage device coupled to the IO  
2 device to transmit data at a data rate higher than the data rate of the low-speed PCI  
3 bus arbiter.

1 22. A system comprising:

2 a first controller having an arbiter to arbitrate requests for a first bus of a  
3 predefined protocol type at a first data rate; and

4 an second controller having:

5 an arbiter to arbitrate requests for a second bus of the predefined protocol  
6 type at a second data rate, wherein the first data rate is at least 10  
7 percent greater than the second data rate; and  
8 control circuitry to interface to the first bus.

1 23. The system of claim 22, further comprising:

2 an IO device coupled to the control circuitry of the second controller without  
3 being coupled to the arbiter of the IO controller.